CLAIMS

We Claim:

1. An integrated circuit having power management comprising:

processing circuitry for executing instructions;

at least one memory array coupled to the processing circuitry for providing data to the processing circuitry; and

control circuitry coupled to the at least one memory array, the control circuitry removing electrical connectivity of the at least one memory array to a supply voltage terminal by firstly disabling all accesses to the at least one memory array and secondly removing electrical power to all of the at least one memory array to reduce leakage current in the at least one memory array.

2. The integrated circuit of claim 1 further comprising:

one or more supporting memory arrays coupled to the at least one memory array, the one or more supporting memory arrays providing a support function to operate the at least one memory array, the control circuitry keeping the one or more supporting memory arrays selectively powered up when electrical power is removed to all of the at least one memory array depending upon whether all data in the at least one memory array must be marked as unusable upon restoring power to the at least one memory array.

3. The integrated circuit of claim 1 wherein the control circuitry further comprises:

a switch having a first terminal coupled to the supply voltage terminal and a second terminal coupled to a power plane terminal of the at least one memory array, the switch further comprising a control terminal for receiving a control signal that determines when the switch is conductive.

4. The integrated circuit of claim 3 wherein the control signal is provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal.

5. The integrated circuit of claim 4 further comprising:
a configuration register for storing a control value that determines whether the control signal is provided in response to execution of the at least one instruction or in response to the power down signal.

6. The integrated circuit of claim 1 further comprising:
a plurality of memory arrays, each of the plurality of memory arrays being coupled to the control circuitry and being able to be independently entirely powered off to reduce transistor leakage current.

7. The integrated circuit of claim 1 further comprising:
a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system memory by flushing the at least one memory array of stored data and physically halts the processing circuitry prior to removing power to the at least one memory array.

8. The integrated circuit of claim 1 further comprising:
a system memory coupled to the processing circuitry, wherein contents of the at least one memory array are synchronized with the system memory and wherein the at least one memory array comprises a copy-back cache that is configured as a write-through cache so that the contents of the at least one memory array are always synchronized with the system memory.

9. The integrated circuit of claim 1 further comprising:
a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system memory by flushing the at least one memory array of stored data prior to disabling accesses to the at least one memory array under control of the processing circuitry for executing instructions and removing power to the at least one memory array.

10. The integrated circuit of claim 9 further comprising:
a control register coupled to the at least one memory array, the control register storing a command signal provided by the processing circuitry for executing

instructions, the command signal disabling accesses to the at least one memory array.

11. The integrated circuit of claim 1 further comprising:

a control register within the control circuitry, the control register receiving and storing a command signal from the processing circuitry for executing instructions that functions to restore power to the at least one memory array, the control circuitry further comprising an array controller that marks all data entries in the at least one memory array with a predetermined bit value prior to the array controller enabling accesses to the at least one memory array.

12. The integrated circuit of claim 1 wherein the control circuitry restores power to the at least one memory array in response to a power up signal and marks all data entries in the at least one memory array as unusable prior to restarting the circuitry for executing instructions.

13. The integrated circuit of claim 1 wherein the control circuitry further comprises monitoring logic that observes memory accesses of the at least one memory array during removing electrical power to all of the at least one memory array, the monitoring logic limiting powering up of the at least one memory array in response to one or more memory requests until a predetermined criteria is met.

14. The integrated circuit of claim 13 wherein the monitoring logic uses differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

15. An integrated circuit having power management comprising:

processing circuitry for executing instructions;

a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane; and

control circuitry coupled to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

16. The integrated circuit of claim 15 wherein the control circuitry provides a control signal to selectively remove electrical connectivity, the control signal being provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal.

17. The integrated circuit of claim 15 wherein the control circuitry halts the processing circuitry prior to removing power from the power supply terminal.

18. The integrated circuit of claim 15 wherein the control circuitry disables access to the plurality of memory bit cells prior to removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

19. The integrated circuit of claim 15 further comprising monitoring logic that observes memory accesses of the memory array during removing electrical power to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the monitoring logic limiting powering up of the memory array peripheral circuitry in response to one or more memory requests until a predetermined criteria is met.

20. The integrated circuit of claim 19 wherein the monitoring logic uses differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

21. A method for reducing leakage current in an integrated circuit comprising:

providing a first power plane of circuitry, the first power plane of circuitry comprising an array of memory cells; and

providing a second power plane of circuitry, the second power plan of circuitry comprising a processor and control circuitry, the control circuitry removing electrical connectivity of the array of memory cells to a supply voltage terminal

by firstly disabling all accesses to the array of memory cells and secondly removing electrical power to all of the array of memory cells to reduce leakage current in the array of memory cells.

22. The method of claim 21 further comprising:

providing at least one supporting array of memory cells in either the first power plane of circuitry or the second power plane of circuitry for providing support functions to the array of memory cells, wherein when the at least one supporting array of memory cells is in the first power plane of circuitry, the supporting array of memory cells is not powered down when the second power plane of circuitry is powered down thereby keeping a record of validity status of bits in the array of memory cells.

23. The method of claim 21 further comprising:

one or more additional power planes of circuitry coupled to the first power plane of circuitry, the one or more additional power planes of circuitry comprising additional arrays of memory cells in which each additional array may be separately and completely powered down independently of whether the second power plane of circuitry is powered.

24. A method of power management in an integrated circuit comprising:

executing instructions with a processor;

providing a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells;

selectively coupling the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells to the power supply terminal for creating a second power plane that is independent of the first power plane;

coupling control circuitry to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells; and

selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

25. The method of claim 24 further comprising:

observing memory accesses of the plurality of memory bit cells during removing of electrical power to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells; and

limiting powering up of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells in response to one or more memory requests until a predetermined criteria is met.

26. The method of claim 25 further comprising:

using differing predetermined criteria depending upon a sequence of instructions executed by the processor.